Trials@uspto.gov
Tel: 571-272-7822

Paper 18
Entered: March 29, 2019

UNITED STATES PATENT AND TRADEMARK OFFICE

---

BEFORE THE PATENT TRIAL AND APPEAL BOARD

---

INTEL CORPORATION,
Petitioner,

v.

INSTITUTE OF MICROELECTRONICS,
CHINESE ACADEMY OF SCIENCES,
Patent Owner.

---

Case IPR2018-01574
Patent 9,070,719 B2

---

Before DONNA M. PRAISS, JO-ANNE M. KOKOSKI, and CHRISTOPHER M. KAISER, *Administrative Patent Judges.*

KAISER, *Administrative Patent Judge*.

# DECISION

Denying Institution of *Inter Partes* Review
*35 U.S.C. § 314*

# INTRODUCTION

## *A. Background*

Intel Corporation ("Petitioner") filed a Petition (Paper 2, "Pet.") requesting an *inter partes* review of claims 1–3, 6, and 7 of U.S. Patent No. 9,070,719 B2 (Ex. 1001, "the '719 patent"). Institute of Microelectronics, Chinese Academy of Sciences ("Patent Owner") filed a Preliminary Response (Paper 11, "Prelim. Resp."). With our authorization, Petitioner filed a Reply to the Preliminary Response (Paper 16, "Reply"), and Patent Owner filed a Sur-Reply (Paper 17, "Sur-Reply").

We have authority to determine whether to institute an *inter partes* review. 35 U.S.C. § 314(b); 37 C.F.R. § 42.4(a). The standard for instituting an *inter partes* review is set forth in 35 U.S.C. § 314(a), which provides that an *inter partes* review may not be instituted unless "there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition."

After considering the Petition, the Preliminary Response, and the evidence of record, we determine that Petitioner has not shown a reasonable likelihood of prevailing with respect to at least one challenged claim. Accordingly, we do not institute *inter partes* review of any claim of the '719 patent on the grounds asserted in the Petition.

## *B. Related Matters*

The parties do not identify any judicial or administrative proceeding that would affect or be affected by a decision in this proceeding. Pet. 3; Paper 3, 1.

*C. The Asserted Grounds of Unpatentability*

Petitioner contends that claims 1–3, 6, and 7 of the '719 patent are unpatentable based on the following grounds (Pet. 30–87):[1]

| Statutory Ground | Basis | Challenged Claim(s) |
|---|---|---|
| § 102 | Liaw[2] | 1, 2, and 6 |
| § 103(a) | Liaw and Kim[3] | 7 |
| § 103(a) | Okuno[4] and Liaw | 1–3 and 6 |
| § 103(a) | Okuno, Liaw, and Kim | 7 |
| § 103(a) | Mandelman[5] and Liaw | 1–3 and 6 |
| § 103(a) | Mandelman, Liaw, and Kim | 7 |
| § 103(a) | Okuno and Chang[6] | 1–3 and 6 |
| § 103(a) | Okuno, Chang, and Kim | 7 |

*D. The '719 Patent*

The '719 patent, titled "Semiconductor Device Structure, Method for Manufacturing the Same, and Method for Manufacturing Fin," issued on June 30, 2015. Ex. 1001, at [45], [54]. The '719 patent relates to "fin transistor structures such as Fin Field Effect Transistors (FinFETs)." *Id.* at 1:27–29. According to the patent, "as device feature sizes are becoming

[1] Petitioner also relies on a Declaration from Dr. Scott Thompson. Ex. 1002.

[2] Liaw et al., U.S. Patent No. 9,362,290 B2, issued June 7, 2016 (Ex. 1003, "Liaw").

[3] Kim et al., US 2006/0175669 A1, published Aug. 10, 2006 (Ex. 1010, "Kim").

[4] Okuno, US 2009/0309141 A1, published Dec. 17, 2009 (Ex. 1005, "Okuno").

[5] Mandelman et al., US 2008/0251934 A1, published Oct. 16, 2008 (Ex. 1006, "Mandelman").

[6] Chang, U.S. Patent No. 7,335,583 B2, issued Feb. 26, 2008 (Ex. 1004, "Chang").

smaller continuously, it is more difficult to make gate electrodes for the fin transistors." *Id.* at 1:66–2:1. In particular, "[a]ccording to the conventional process," after a gate line is cut into separate gate electrodes, "processes such as dielectric spacer formation should be performed." *Id.* at 5:1–3. This "conventional process" is illustrated in Figure 8 of the '719 patent, which is reproduced below:

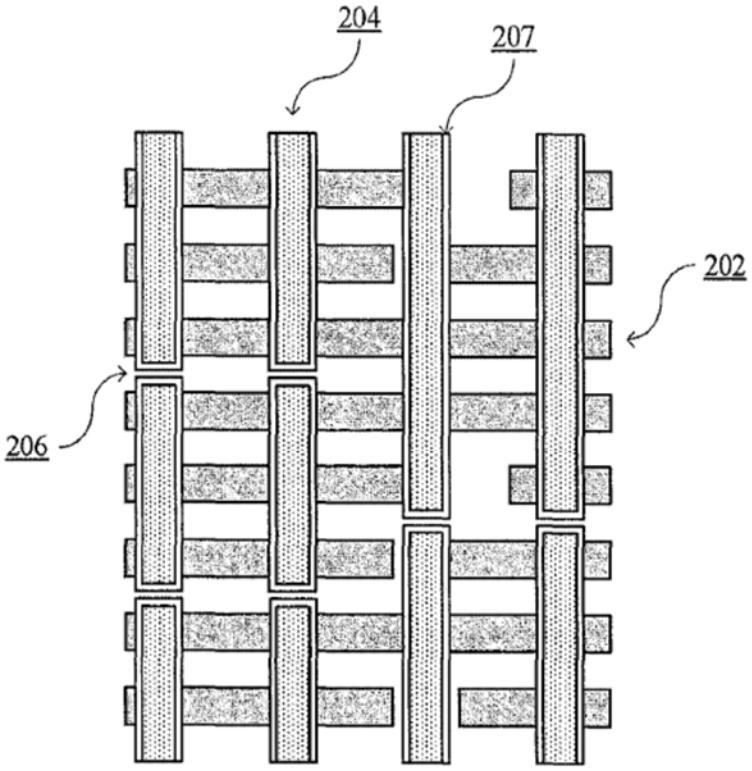
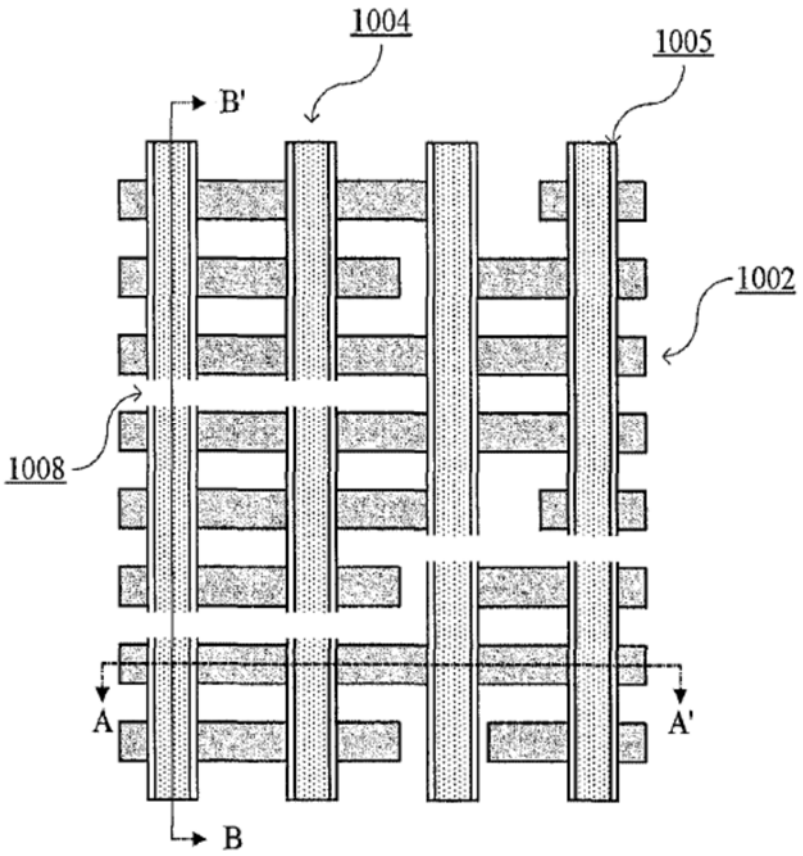



Fig. 8

*Id.* at Fig. 8. Figure 8 "is a diagram schematically showing a gate electrode and a gate spacer surrounding the gate electrode as a result of the conventional process." *Id.* at 3:13–15. In Figure 8, several gate electrodes 204 cross several fins 202, with dielectric spacers 207 "surrounding the respective gate electrodes." *Id.* at 5:3–5. Because the dielectric spacers

surround each gate electrode separately, "the material of the spacers will enter into the cuts 206" between the gate electrodes. *Id.* at 5:10–12. The '719 patent notes that forcing the dielectric material into these cuts "will impact the profile of the dielectric spacers," potentially causing voids to form in the dielectric material that may "cause defects such as shorts in subsequent processes." *Id.* at 5:12–20.

The '719 patent describes a process for avoiding the problems that can be caused by the conventional process. *Id.* at 5:29–30. This process involves forming a dielectric spacer layer surrounding the gate lines before the gate lines "are cut off at predetermined positions . . . to achieve inter-device electrical isolations." *Id.* at 6:11–48. The result of this process is depicted in Figure 11(a) of the '719 patent, which is reproduced below:



*Id.* at Fig. 11. Figure 11(a) "is a top view" of one step in "a process flow for manufacturing a semiconductor device structure according to a first embodiment of the present disclosure." *Id.* at 3:16–20. In Figure 11(a), several gate electrodes 1004 cross several fins 1002. Each gate electrode has dielectric spacer 1005 on its long lateral surfaces, with no dielectric spacer located in cuts 1008 that separate the gate electrodes. *Id.* at 6:44–51.

*E. Illustrative Claim*

Claims 1–3, 6, and 7 of the '719 patent are challenged. Claim 1 is independent and illustrative; it recites:

> 1. A method for manufacturing a semiconductor device structure, comprising:
>
> forming a fin in a first direction on a semiconductor substrate;
>
> forming a gate line in a second direction, the second direction crossing the first direction on the semiconductor substrate, and the gate line intersecting the fin with a gate dielectric layer sandwiched between the gate line and the fin;
>
> forming a dielectric spacer surrounding the gate line; and
>
> performing inter-device electrical isolation at a predetermined position after forming the dielectric spacer, wherein isolated portions of the gate line form independent gate electrodes of respective devices.

Ex. 1001, 10:19–32.

## ANALYSIS

*A. Claim Construction*

In an *inter partes* review, we construe claim terms in an unexpired patent according to their broadest reasonable construction in light of the

specification of the patent in which they appear.[7] 37 C.F.R. § 42.100(b) (2016). Claim terms generally are given their ordinary and customary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). Only terms which are in controversy need to be construed, and then only to the extent necessary to resolve the controversy. *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999).

Petitioner does not request an explicit construction for any of the claim terms. Patent Owner argues that we should construe the term "a dielectric spacer surrounding the gate line." Prelim. Resp. 9–10. Specifically, Patent Owner argues that we should interpret this phrase as "forming a dielectric spacer enclosing the gate line on all side surfaces." *Id.* Petitioner does not argue to the contrary, Pet. 1–87, and Petitioner appears tacitly to accept this construction, because Petitioner argues that the asserted prior-art references disclose the formation of dielectric spacers enclosing gate lines on all side surfaces. *See, e.g.*, Pet. 34 ("Because sidewall spacers on the long lateral sides and the ends of the gate line are on substantially vertical surfaces, the etching technique disclosed in Liaw and Mandelman [which removes material from horizontal surfaces while leaving material in place on vertical surfaces] resulted in sidewall spacers surrounding the gate lines."). Moreover, Patent Owner's proposed construction is consistent with

[7] A recent amendment to this rule does not apply here, because the Petition was filed before November 13, 2018. *See* "Changes to the Claim Construction Standard for Interpreting Claims in Trial Proceedings Before the Patent Trial and Appeal Board," 83 Fed. Reg. 51,340 (Oct. 11, 2018) (to be codified at 37 C.F.R. pt. 42).

the language of the '719 patent. Ex. 1001, 6:18–21 ("dielectric spacer layer 1005 is formed on opposite lateral outer sides of the respective gate lines 1004 in the horizontal direction of the figure, besides those formed at the ends of the gate lines 1004 in the vertical direction of the gate line"). Accordingly, on the present record, we adopt Patent Owner's proposed construction, and we interpret "a dielectric spacer surrounding the gate line" as "forming a dielectric spacer enclosing the gate line on all side surfaces."

*B. Alleged Anticipation by Liaw*

Petitioner argues that claims 1, 2, and 6 of the '719 patent are anticipated by Liaw. Pet. 30–38.

*1. Liaw*

Liaw relates to "[a] system and method for a memory cell layout." Ex. 1003, at [57]. According to Liaw, "[f]undamental limitations involved with the lithographic process limit its usefulness in forming fins and gate electrodes as FinFETs are scaled to smaller and smaller dimensions." *Id.* at 1:28–34. Liaw discloses a means of "solv[ing] or circumvent[ing]" this problem by manufacturing "an SRAM cell layout . . . using dummy layers and spacers." *Id.* at 1:41–44. As an optional step in its process, Liaw discloses "the formation of permanent spacers . . . by blanket depositing a spacer layer" and then "anisotropically etching to remove the spacer layer from the horizontal surfaces of the structure." *Id.* at 7:25–38. Similarly, Liaw discloses forming "first spacers 211 . . . by blanket depositing a spacer layer . . . over the previously formed structure" and then "anisotropically etching and removing the spacer layer 210 from the horizontal surfaces of the structure." *Id.* at 3:61–4:6. Although Liaw does not illustrate the optional step of forming permanent spacers, *id.* at 7:25–26, it does illustrate

the formation of first spacers 211. This process is illustrated in Figures 2B and 2C, which are reproduced below:

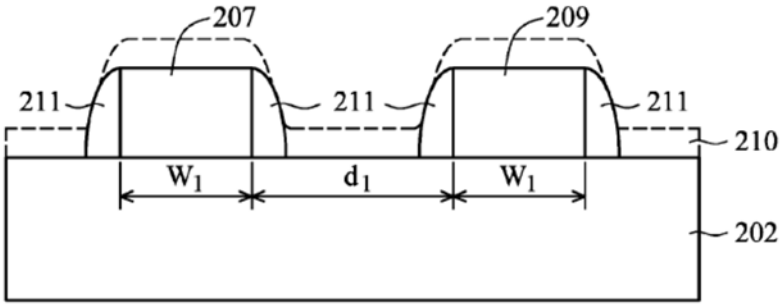



Figure 2B

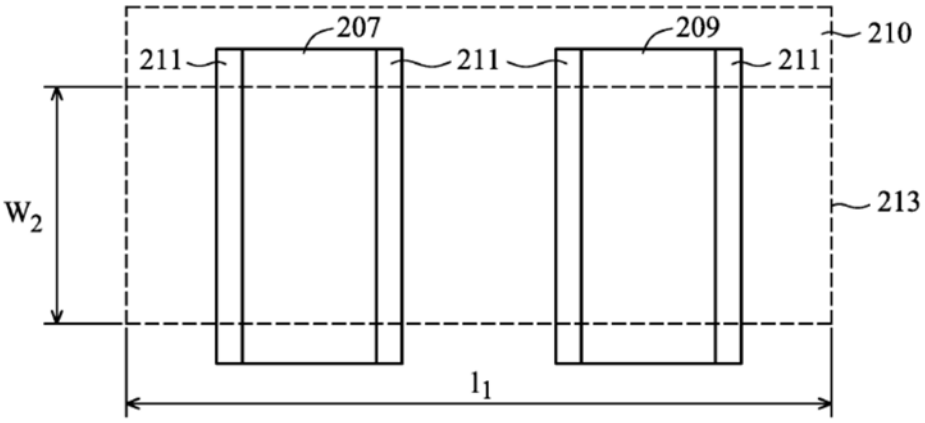



Figure 2C

*Id.* at Figs. 2B, 2C. Figures 2B and 2C depict a portion of a process for forming "a fin in accordance with an embodiment" of Liaw. *Id.* at 2:20–21. Specifically, these figures "illustrate a cross-sectional view and a plan view, respectively, of the formation of a first dummy layer 207, a second dummy layer 209, and first spacers 211." *Id.* at 3:34–36. Figure 2B depicts the blanket deposition of spacer layer 210 over dummy layers 207 and 209, and Figure 2C depicts spacer layer 210 covering both the long lateral surfaces and the end faces of dummy layers 207 and 209. *Id.* at 3:61–65. Figures 2B and 2C both depict spacers 211, created by anisotropically etching spacer

layer 210, only on the long lateral surfaces of dummy layers 207 and 209, and not on the end faces of those layers. *Id.* at 4:4–6.

*2. Analysis*

Independent claim 1 recites "forming a dielectric spacer surrounding the gate line." Ex. 1001, 10:19–32. As discussed above, we interpret this limitation as "forming a dielectric spacer enclosing the gate line on all side surfaces." Thus, claim 1 requires the formation of a dielectric spacer on all side surfaces of the gate line, including both the long lateral surfaces of the gate line and the end faces of the gate line.[8] Because claims 2 and 6 depend from claim 1, they include the limitations of claim 1. 37 C.F.R. § 1.75(c); Ex. 1001, 10:33–51.

Petitioner argues that Liaw discloses the formation of such a dielectric spacer. Pet. 33–34. Specifically, Petitioner argues that Liaw's disclosure of "the formation of permanent spacers" by "blanket depositing a spacer layer" and then anisotropically etching that layer is a disclosure of the formation of a dielectric spacer on all side surfaces of the gate line. *Id.* at 33 (citing Ex. 1002 ¶¶ 222–223; Ex. 1003, 7:25–38). According to Petitioner, the "blanket deposition [disclosed in Liaw] placed sidewall spacer material on all sides of the gate line," and the removal of material by anisotropic etching

[8] A gate line or similar raised rectangular structure built on the upper surface of a substrate has four lateral surfaces: two long lateral surfaces, which Petitioner refers to as "long lateral sides," Pet. 34, and two short lateral surfaces at right angles to the long lateral surfaces. To avoid confusion, except when quoting evidence or filings in this proceeding, we refer to the long lateral surfaces as "long lateral surfaces" and to the short lateral surfaces as "end faces." When referring collectively to the collection of all short and long lateral surfaces, we use the term "all side faces."

removed material only from the horizontal surfaces, leaving material on both the long lateral surfaces and the end faces of the gate line. *Id.* Moreover, Petitioner argues, the fact that the Liaw process of blanket deposition followed by anisotropic etching is the same as the process described in the '719 patent for forming dielectric spacers means that the Liaw process must produce the same result as the '719 patent's process: a dielectric spacer surrounding the gate line. *Id.* at 33–34 (citing Ex. 1001, 6:11–17, 8:5; Ex. 1002 ¶¶ 224–229).

Patent Owner argues that Petitioner has not shown sufficiently that Liaw's permanent spacers surround Liaw's gate line. Prelim. Resp. 13–15. Specifically, Patent Owner argues that Petitioner has not shown sufficiently that, in Liaw's process, permanent spacers are formed on the end surfaces of the gate line. *Id.*

We agree with Patent Owner. Petitioner's argument rests on the idea that all processes that involve blanket deposition of a dielectric spacer layer over a gate line followed by anisotropic etching to remove spacer material from horizontal surfaces will result in spacer material being present on the vertical end faces of the gate line. Pet. 33–34. For example, Dr. Thompson, Petitioner's declarant, testifies that "[b]lanket deposition [in general] is a process in which the sidewall spacer material is laid across the entire circuit structure, including around all sides of and on top of any gate line found on top of the substrate." Ex. 1002 ¶ 223. Dr. Thompson also testifies that "[t]he term 'blanket' is used because the sidewall spacer material covers every exposed surface in the semiconductor substrate being processed." *Id.* Because the material is placed on every surface, and because anisotropic etching removes the material only from the horizontal surfaces of the

structure, Dr. Thompson testifies that the process of blanket deposition followed by anisotropic etching must leave spacer material on all vertical surfaces, including the end faces of the gate line. *Id.*

But Liaw itself contradicts this testimony. Liaw discloses a method for forming "first spacers 211" on dummy layers 207 and 209. Ex. 1003, 3:61–4:6, Figs. 2B, 2C. As with Liaw's process for forming permanent spacers, on which Petitioner relies, this process involves "blanket depositing a spacer layer over the previously formed structure," and "anisotropically etching and removing the spacer layer 210 from the horizontal surfaces of the structure." *Id.* at 3:61–4:6. The blanket deposition covers at least one end of each dummy layer. *Id.* at Fig. 2C (depicting spacer layer 210 as covering one end of dummy layers 207 and 209). The spacers formed by this process, however, are formed only on the long lateral surfaces of the dummy layers, and not on the end faces of the dummy layers. *Id.* at Figs. 2C, 2E, 2G. Thus, despite Dr. Thompson's testimony, it is not necessarily the case that all processes involving blanket deposition of spacer material over a gate line followed by anisotropic etching of that material necessarily leave spacer material on all side surfaces of the gate line, including the end faces. Accordingly, simply showing that Liaw discloses a process of spacer formation in which spacer material is blanket deposited over a gate line and then anisotropically etched is not sufficient to show that Liaw discloses a process of spacer formation that results in spacer material being placed on all side surfaces of the gate line.

Because Petitioner has not shown sufficiently that Liaw discloses "forming a dielectric spacer surrounding the gate line," we conclude that Petitioner has not established a reasonable likelihood of prevailing in

showing the unpatentability either of claim 1 or of claims 2 and 6, which depend from claim 1, as anticipated by Liaw.

*C. Alleged Obviousness over Liaw and Kim*

Petitioner argues that claim 7 of the '719 patent would have been obvious over the combination of Liaw and Kim. Pet. 39–43.

*1. Kim*

Kim relates to "a semiconductor device including a FinFET having a metal gate electrode and a fabricating method thereof." Ex. 1010, at [57]. Specifically, Kim teaches "a method of fabricating a semiconductor device" that involves "forming a dummy gate electrode," "forming a gate spacer on a sidewall of the dummy gate electrode," "removing the dummy gate electrode," and then "forming a metal gate electrode in an area in which the dummy gate electrode is removed." *Id.* ¶ 11.

*2. Analysis*

Claim 7 depends from claim 1. Ex. 1001, 10:52–56. Accordingly, claim 7 includes all the limitations of claim 1. 37 C.F.R. § 1.75(c). Petitioner argues that Liaw teaches all the limitations of claim 1. Pet. 41 ("Liaw taught all the limitations of claim 1"). As discussed above, however, we conclude that Petitioner has not shown sufficiently that Liaw teaches or suggests "forming a dielectric spacer surrounding the gate line."

Petitioner also argues that Kim teaches or suggests this limitation.[9] *Id.* at 42 ("[L]ike Liaw, Kim taught the FinFET structures required by

[9] Petitioner's argument regarding Kim teaching "forming a dielectric spacer surrounding the gate line" arguably violates our rule against incorporation by reference, 37 C.F.R. § 42.6(a)(3), because Petitioner does not explain how Kim teaches this limitation. Instead, Petitioner merely cites to allegedly

claim 1—fins, gate lines, gate dielectric layers, and dielectric spacers.") (citing Ex. 1010, at [57], ¶¶ 10–11, claims 1, 4). Petitioner is correct that Kim teaches "sidewall spacers." *E.g.*, Ex. 1010, at [57] ("The semiconductor device includes . . . a gate spacer formed on a sidewall of the metal gate electrode"), ¶¶ 10 ("a semiconductor device including . . . a gate spacer formed on a sidewall of the metal gate electrode"), 11 ("a method of fabricating a semiconductor device, including . . . forming a gate spacer on a sidewall of the dummy gate electrode"). But every portion of Kim cited by Petitioner teaches forming a gate spacer "on a sidewall of the . . . gate electrode." *Id.* at [57], ¶¶ 10, 11, claims 1, 4. The formation of a spacer on a sidewall of an electrode is not necessarily the formation of a dielectric spacer surrounding the gate line. Accordingly, Petitioner has not shown sufficiently that Kim teaches or suggests "forming a dielectric spacer surrounding the gate line."

Because Petitioner has not shown sufficiently that either Liaw or Kim teaches "forming a dielectric spacer surrounding the gate line," and because claim 7 contains this limitation through its dependence from claim 1, we conclude that Petitioner has not established a reasonable likelihood of prevailing in showing the unpatentability of claim 7 as obvious over the combination of Liaw and Kim.

*D. Alleged Obviousness over Okuno and Liaw*

Petitioner argues that claims 1–3 and 6 of the '719 patent would have been obvious over the combination of Okuno and Liaw. Pet. 43–56.

---

relevant portions of Kim. Pet. 42; *see also* Pet. 71, 86 (repeating same argument). We address the argument here, however, for the sake of completeness.

*1. Okuno*

Okuno "is directed to a semiconductor device and a manufacturing method of the same." Ex. 1005 ¶ 2. In Okuno's process, a "straight and continuous" gate electrode 25 is formed. *Id.* ¶ 26, Fig. 6A. After the gate electrode is formed, "pocket implantation is performed . . . so as to form pocket regions 26" on both sides of the gate electrode. *Id.* ¶ 26, Fig. 6B. "Next, extension implantation is performed, as the gate electrode 25 still remains continuous, so as to form sidewall spacers" 27. *Id.* ¶ 26, Fig. 6C. After these steps, and after "source/drain implantation is performed," "the gate is cut and divided to form gate electrodes in designed shapes." *Id.* ¶ 26. Okuno states that its sidewall spacers 27 "are provided only in the longitudinal direction of the gate (i.e. along the gate length direction)." *Id.* ¶ 28. Although Okuno describes its sidewall spacers as formed via "extension implantation," *id.* ¶ 26, it also describes them as "formed, for example, of a CVD oxide film having a thickness of 30 to 80 nm." *Id.* ¶ 33.

Okuno illustrates its sidewall spacers 27 in two drawings, Figures 6C and 7B, which are reproduced below:

FIG.6C

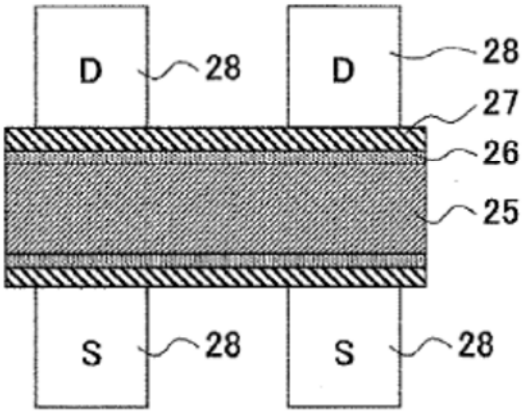
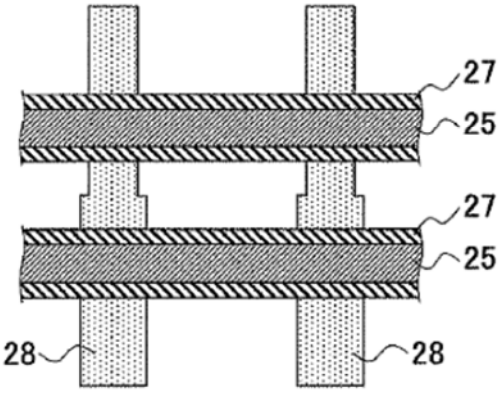



FIG.7B



*Id.* at Figs. 6C, 7B. Figure 6C illustrates one step of "a basic concept of the present disclosure," and Figure 7B illustrates one step of a "manufacturing process[] of a semiconductor device according to one embodiment of the present disclosure." *Id.* ¶¶ 20–21. In Figure 6C, "straight and continuous" gate electrode 25 overlays source and drain regions 28, with pocket regions 26 formed immediately adjacent to the long lateral surfaces of the gate electrode and sidewall spacers 27 formed immediately adjacent to the pocket regions. *Id.* ¶ 26. In Figure 7B, "straight and continuous" gate electrodes 25 overlay source and drain regions 28, with sidewall spacers 27 formed immediately adjacent to the long lateral surfaces of the gate electrodes. *Id.* ¶¶ 32–33. Wavy lines at the ends of each gate electrode suggest that the depicted structure continues beyond the left and right edges of the illustration.

*2. Analysis*

Independent claim 1 recites "forming a dielectric spacer surrounding the gate line." Ex. 1001, 10:19–32. Claims 2, 3, and 6 all depend from claim 1, so they include the same limitation. 37 C.F.R. § 1.75(c); Ex. 1001, 10:33–51. Petitioner argues that both Okuno and Liaw teach or suggest this limitation. Pet. 49–51. As discussed above with respect to the Liaw anticipation ground, Petitioner has not shown sufficiently that Liaw discloses "forming a dielectric spacer surrounding the gate line," because it is unclear whether Liaw's dielectric spacer is formed on the end faces of the gate line, as opposed to only on its long lateral surfaces.

As for Okuno, the parties dispute whether Okuno's sidewall spacers 27 are dielectric spacers of the type recited in the challenged claims, or whether they are instead extension implantation regions buried in the

substrate. Pet. 49–52; Prelim. Resp. 23–26; Reply 1–6; Sur-Reply 1–4. On the present record, it is unclear which party is correct in its interpretation of Okuno. There is language in Okuno suggesting that sidewall spacers 27 are formed by implantation into the substrate. Ex. 1005 ¶ 26 ("extension implantation is performed . . . so as to form sidewall spacers . . ."). But there also is language suggesting that the sidewall spacers are formed of an oxide film deposited on top of the substrate. *Id.* ¶ 33 ("sidewalls 27 formed, for example, of a CVD oxide film having a thickness of 30 to 80 nm."). We need not resolve the question of whether Okuno's sidewall spacers are structures within or built on the top surface of the substrate. As discussed below, even assuming that Okuno's sidewall spacers are built on the top surface of the substrate, we conclude that Petitioner has not shown sufficiently that those spacers are present on all side faces of the gate lines, including the end faces.

On the present record, Okuno itself suggests that spacer material is not present on the end faces of its gate lines. Both Figure 6C and Figure 7B depict only spacers[10] formed on the long lateral surfaces of the gate electrodes, without depicting the end faces of those lines, which is at best ambiguous evidence that could not prove either the presence or the absence of spacer material on the end faces of the gate lines. Ex. 1005, Figs. 6C, 7B. Accordingly, these figures do not themselves depict spacer material enclosing the gate line on all side surfaces. Petitioner argues that Figure 7B

[10] The parties dispute whether Okuno's sidewall spacers 27 are dielectric spacers of the type recited in the challenged claims or whether they are instead extension implantation regions buried in the substrate. Pet. 49–52; Prelim. Resp. 23–26; Reply 1–6; Sur-Reply 1–4. On the present record, it is unclear which party is correct in its interpretation of Okuno.

supports the argument that spacer material is present on the end faces of the lines by noting that the "curvilinear ends" on the gate lines in Figure 7B "indicate that the gate lines continue to the left and right." Pet. 50 (citing Ex. 1002 ¶ 266). Petitioner is correct that Figure 7B indicates the continuation of the gate lines beyond the edges of the illustration, but the fact that the gate lines continue beyond the edges of the illustration says nothing about the presence or absence of spacer material on the end faces of the gate lines. Moreover, Okuno states that its sidewall spacers "are provided only in the longitudinal direction of the gate (i.e. along the gate length direction)," which is evidence that the spacers actually are not placed on the end faces of the gate lines. Ex. 1005 ¶ 28.

As it argued with respect to Liaw, Pet. 33, Petitioner argues that Okuno teaches using a deposition process to form its sidewall spacers that will always result in spacer material covering the end faces of the gate lines as well as their long lateral surfaces. *Id.* at 49. Specifically, Petitioner argues that "[a] person of skill in the art would have understood that" the CVD oxide film of Okuno "would cover the entire surface of the semiconductor substrate, including the long sides and ends of the gate lines." *Id.* (citing Ex. 1002 ¶¶ 265–266). This argument is supported by the testimony of Dr. Thompson, who testifies that "the conventional CVD . . . technique used to form the dielectric oxide sidewall spacers on the sidewalls of the gate lines in Okuno" would always result in "sidewall spacers [being] formed on all sides of the gate line, both the lateral sides and the end faces." Ex. 1002 ¶ 266. As discussed above with respect to the Liaw anticipation ground, however, the disclosure of Liaw makes clear that not all processes involving blanket deposition of spacer material over gate lines followed by

anisotropic etching necessarily result in spacer material being present on the end faces of the gate lines. Ex. 1003, 3:61–4:6, Figs. 2B, 2C, 2E, 2G; Section B.2, *supra*. Accordingly, simply showing that Okuno discloses a process of spacer formation in which spacer material is blanket deposited over a gate line and then anisotropically etched is not sufficient to show that Okuno teaches or suggests a process of spacer formation that results in spacer material being placed on all side surfaces of the gate line.

Thus, Petitioner has not shown sufficiently that either Okuno or Liaw teaches or suggests "forming a dielectric spacer surrounding the gate line." Because claims 1–3 and 6 all include this limitation directly or through their dependence from claim 1, we conclude that Petitioner has not established a reasonable likelihood of prevailing in showing the unpatentability of claims 1–3 and 6 as obvious over the combination of Okuno and Liaw.

*E. Alleged Obviousness over Okuno, Liaw, and Kim*

Petitioner argues that claim 7 of the '719 patent would have been obvious over the combination of Okuno, Liaw, and Kim. Pet. 56–57. Claim 7 depends from claim 1. Ex. 1001, 10:52–56. Accordingly, claim 7 includes all the limitations of claim 1. 37 C.F.R. § 1.75(c). Petitioner relies on the combination of Okuno and Liaw to teach all the limitations of claim 1, including the "forming a dielectric spacer surrounding the gate line" limitation discussed above. Pet. 56 ("Okuno in combination with Liaw taught all the limitations of claim 1"). Petitioner does not argue in the context of the combination of the teachings of Okuno, Liaw, and Kim that Kim also teaches or suggests this limitation. *Id.* at 56–57. Moreover, as discussed above, we are not persuaded by Petitioner's argument with respect to the proposed combination of Liaw and Kim that Petitioner has shown

sufficiently that Kim teaches or suggests this limitation. *See* Section C.2, *supra*.

Because Petitioner has not shown sufficiently that Okuno, Liaw, or Kim teaches "forming a dielectric spacer surrounding the gate line," and because claim 7 contains this limitation, we conclude that Petitioner has not established a reasonable likelihood of prevailing in showing the unpatentability of claim 7 as obvious over the combination of Okuno, Liaw, and Kim.

*F. Alleged Obviousness over Mandelman and Liaw*

Petitioner argues that claims 1–3 and 6 would have been obvious over the combination of Mandelman and Liaw. Pet. 57–68.

*1. Mandelman*

Mandelman relates to "improved semiconductor device structures and methods used to interconnect the transistors in a conventional [static RAM] memory cell while simultaneously either reducing the number of CA contacts or completely eliminating CA contacts." Ex. 1006 ¶ 10. In Mandelman's method, sidewall spacers are formed on conductor lines that overlay active semiconductor regions. *Id.* ¶¶ 24–29. This process is depicted in Figure 2 of Mandelman, which is reproduced below:

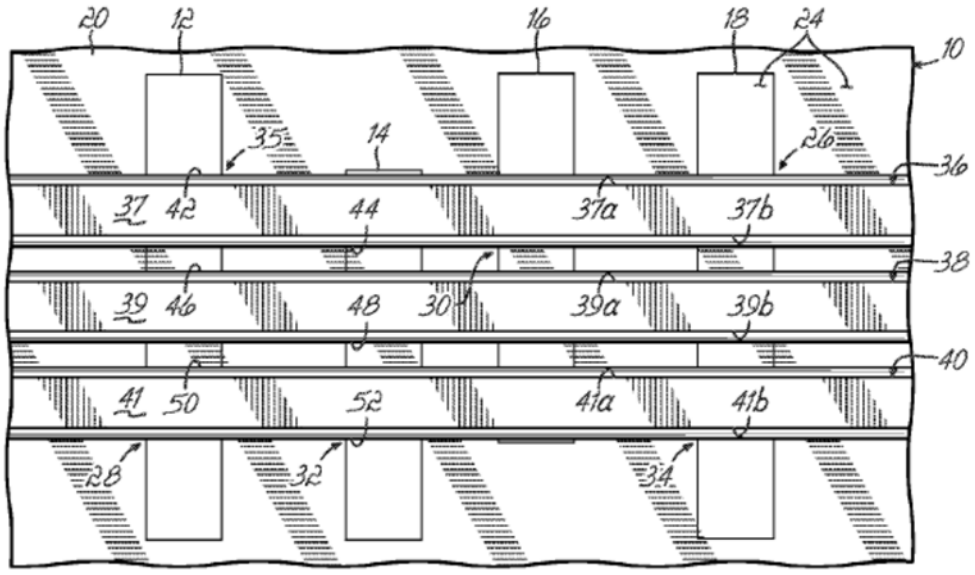



FIG. 2

*Id.* at Fig. 2. Figure 2 depicts a cross-sectional view of a portion of a substrate at one stage of "a processing method in accordance with an embodiment of the invention" of Mandelman. *Id.* ¶ 15. Conductor lines 36, 38, 40 overlay active semiconductor regions 12, 14, 16, 18. *Id.* ¶¶ 24–27, 29, Fig. 2. Sidewall spacers 42, 44, 46, 48, 50, 52 "are formed on the sidewalls" of conductor lines 36, 38, 40. *Id.* ¶ 29. The sidewalls of each conductor line are indicated in Figure 2. For example, the sidewalls of conductor line 36 are depicted as 37a and 37b, with sidewall spacer 42 immediately adjacent to sidewall 37a and sidewall spacer 44 immediately adjacent to sidewall 37b.

*2. Analysis*

Each of claims 1–3 and 6 contains a limitation requiring "forming a dielectric spacer surrounding the gate line." Ex. 1001, 10:19–51. Petitioner

argues that both Mandelman and Liaw teach or suggest this limitation.[11] Pet. 62–64. As discussed above with respect to the Liaw anticipation ground, Petitioner has not shown sufficiently that Liaw discloses "forming a dielectric spacer surrounding the gate line," because it is unclear whether Liaw's dielectric spacer is formed on the end faces of the gate line, as opposed to only on its long lateral surfaces. Section B.2, *supra*. We find the same to be true with respect to Mandelman.

On the present record, Mandelman itself suggests that spacer material is not present on the end faces of its gate lines. First, Figure 2 of Mandelman is ambiguous in the same way that Figures 6C and 7B of Okuno are ambiguous, because it does not depict the end faces of the gate lines, providing no evidence as to either the presence or absence of spacer material in those locations. Ex. 1006, Fig. 2. Second, Mandelman identifies each gate line as having sidewall spacers only on two lateral surfaces, not the four lateral surfaces that would be expected if spacer material were present on both the long lateral surfaces and both the end faces. *Id.* ¶ 29 ("sidewall spacers are formed on the sidewalls 37a,b of conductor line 36"), Fig. 2. This is evidence that the spacers actually are not placed on the end faces of the gate lines.

As it did with the similar problems in Okuno and Liaw, Petitioner tries to overcome this problem with Mandelman by arguing that Mandelman teaches using a deposition process to form its sidewall spacers that will

[11] Although the portion of the Petition relating to this asserted ground does not contain any argument that Liaw teaches or suggests "forming a dielectric spacer surrounding the gate line," Pet. 62–64, Petitioner argues in other portions of the Petition that Liaw teaches or suggests this limitation. *See, e.g.*, *id.* at 33–34, 49–52.

always result in spacer material covering the end faces of the gate lines as well as their long lateral surfaces. Pet. 62–63. Specifically, Petitioner argues that Mandelman's deposition of "a blanket layer" would always "create spacer material on all sides of the gate line," and Mandelman's "reactive ion etching" would "'remove[] portions of the blanket dielectric layer from substantially horizontal surfaces at a faster rate than from substantially vertical surfaces.'" *Id.* (quoting Ex. 1006 ¶ 29; citing Ex. 1002 ¶¶ 316–318). As discussed above with respect to Okuno and Liaw, this argument relies on the presumed fact that all processes involving blanket deposition followed by anisotropic etching necessarily result in the deposited material being placed on and remaining on all vertical surfaces. *See* Section D.2, *supra*. But, as also discussed above, Liaw teaches a process of blanket deposition followed by anisotropic etching that does not result in the presence of the deposited material on all vertical surfaces. Ex. 1003, 3:61–4:6, Figs. 2B, 2C, 2E, 2G; Section B.2, *supra*. Accordingly, simply showing that Mandelman discloses a process of spacer formation in which spacer material is blanket deposited over a gate line and then anisotropically etched is not sufficient to show that Mandelman teaches or suggests a process of spacer formation that results in spacer material being placed on all side surfaces of the gate line.

Thus, Petitioner has not shown sufficiently that either Mandelman or Liaw teaches or suggests "forming a dielectric spacer surrounding the gate line." Because claims 1–3 and 6 all contain this limitation, we conclude that Petitioner has not established a reasonable likelihood of prevailing in showing the unpatentability of claims 1–3 and 6 as obvious over the combination of Mandelman and Liaw.

*G. Alleged Obviousness over Mandelman, Liaw, and Kim*

Petitioner argues that claim 7 of the '719 patent would have been obvious over the combination of Mandelman, Liaw, and Kim. Pet. 68–72. Claim 7 depends from claim 1. Ex. 1001, 10:52–56. Accordingly, claim 7 includes all the limitations of claim 1. 37 C.F.R. § 1.75(c). Petitioner argues that the combination of Mandelman and Liaw teaches all the limitations of claim 1. Pet. 70 ("Mandelman and Liaw taught all limitations in claim 1"). As discussed above, however, we conclude that Petitioner has not shown sufficiently that either Mandelman or Liaw teaches or suggests "forming a dielectric spacer surrounding the gate line."

Petitioner also argues that Kim teaches or suggests this limitation, repeating the argument it offers with respect to the Liaw/Kim ground. *Compare id.* at 71 ("Like Liaw, Kim taught the FinFET structures recited in claim 1—fins, gate lines, gate dielectric layers, and sidewall spacers."), *with id.* at 42 ("[L]ike Liaw, Kim taught the FinFET structures required by claim 1—fins, gate lines, gate dielectric layers, and dielectric spacers."). As discussed above, we are not persuaded by this argument that Petitioner has shown sufficiently that Kim teaches or suggests "forming a dielectric spacer surrounding the gate line."

Because Petitioner has not shown sufficiently that Mandelman, Liaw, or Kim teaches "forming a dielectric spacer surrounding the gate line," and because claim 7 contains this limitation, we conclude that Petitioner has not established a reasonable likelihood of prevailing in showing the unpatentability of claim 7 as obvious over the combination of Mandelman, Liaw, and Kim.

*H. Alleged Obviousness over Okuno and Chang*

Petitioner argues that claims 1–3 and 6 would have been obvious over the combination of Okuno and Chang. Pet. 72–83.

*1. Chang*

Chang "relate[s] generally to semiconductor processing and more specifically to methods for isolating semiconductor structures." Ex. 1004, 1:6–8. Chang's method "forms a grid of continuous parallel gate electrode structures overlaying a grid of continuous parallel diffusion regions," with those grids being "perpendicular to each other," forming "an overlapping array." *Id.* at 2:28–37. After the grids are formed, Chang teaches "selectively removing specific interconnecting gate electrode regions" and replacing the "removed material . . . with a dielectric material" in order to isolate individual transistors from one another. *Id.* at 2:43–55. In some embodiments of Chang, "the substrate surface [is not] planar," permitting "subsequently patterned gate electrodes [to] wrap around the top and sidewalls of the diffusion regions, thereby forming tri-gates or similar structures." *Id.* at 3:25–30.

*2. Analysis*

Each of claims 1–3 and 6 contains a limitation requiring "forming a dielectric spacer surrounding the gate line." Ex. 1001, 10:19–51. Petitioner argues that Okuno teaches or suggests this limitation. Pet. 77–79. As discussed above with respect to the proposed combination of Okuno and Liaw, Petitioner has not shown sufficiently that Okuno teaches or suggests "forming a dielectric spacer surrounding the gate line," because it is unclear whether Okuno's dielectric spacer is formed on the end faces of the gate line, as opposed to only on its long lateral surfaces. Petitioner does not

argue that Chang teaches or suggests this limitation.[12] *Id.* Accordingly, we conclude that Petitioner has not established a reasonable likelihood of prevailing in showing the unpatentability of claims 1–3 and 6 as obvious over the combination of Okuno and Chang.

*I. Alleged Obviousness over Okuno, Chang, and Kim*

Petitioner argues that claim 7 of the '719 patent would have been obvious over the combination of Okuno, Chang, and Kim. Pet. 83–87. Claim 7 depends from claim 1. Ex. 1001, 10:52–56. Accordingly, claim 7 includes all the limitations of claim 1. 37 C.F.R. § 1.75(c). Petitioner argues that the combination of Okuno and Chang teaches all the limitations of claim 1. Pet. 86 ("Okuno and Chang taught all limitations of claim 1"). As discussed above, however, we conclude that Petitioner has not shown sufficiently that either Okuno or Chang teaches or suggests "forming a dielectric spacer surrounding the gate line."

Petitioner also argues that Kim teaches or suggests this limitation, repeating the argument it offers with respect to the Liaw/Kim ground. *Compare id.* ("Like Chang, Kim taught the FinFET structures recited in claim 1—fins, gate lines, gate dielectric layers, and sidewall spacers."), *with id.* at 42 ("[L]ike Liaw, Kim taught the FinFET structures required by claim

[12] In discussing the Okuno/Chang/Kim ground, Petitioner states in passing that "Chang . . . taught the FinFET structures recited in claim 1—fins, gate lines, gate dielectric layers, and sidewall spacers." Pet. 86. But Petitioner does not explain in that portion of the Petition how Chang teaches sidewall spacers that surround the gate lines, nor does Petitioner even cite to Chang to support this statement. *Id.* In the portion of the Petition discussing the Okuno/Chang ground, Petitioner does not argue, much less show sufficiently, that Chang teaches "forming a dielectric spacer surrounding the gate line." *Id.* at 77–79.

1—fins, gate lines, gate dielectric layers, and dielectric spacers."). As discussed above, we are not persuaded by that Petitioner has shown sufficiently that Kim teaches or suggests "forming a dielectric spacer surrounding the gate line."

Because Petitioner has not shown sufficiently that Okuno, Chang, or Kim teaches "forming a dielectric spacer surrounding the gate line," and because claim 7 contains this limitation, we conclude that Petitioner has not established a reasonable likelihood of prevailing in showing the unpatentability of claim 7 as obvious over the combination of Okuno, Chang, and Kim.

## CONCLUSION

Upon consideration of the Petition, the Preliminary Response, and the evidence before us, we determine that Petitioner has not shown a reasonable likelihood of prevailing with respect to at least one challenged claim. Accordingly, we do not institute *inter partes* review of any challenged claim.

## ORDER

It is hereby

ORDERED that, pursuant to 35 U.S.C. § 314, the Petition is denied, and no *inter partes* review is instituted.

PETITIONER:

Jonathan McFarland
Chad Campbell
Tyler Bowen
PERKINS COIE LLP
Intel-IMECAS-Service-IPR@perkinscoie.com

PATENT OWNER:

David C. Radulescu, Ph.D.
Jonathan Auerbach
Etai Lahav
RADULESCU LLP
david@radip.com
jonathan@radip.com
etai@radulescullp.com